REMARKS

In response to the Office Action mailed August 12, 2005, Applicants respectfully request reconsideration of the Application in view of the foregoing Amendments and the following Remarks. The claims as now presented are believed to be in allowable condition.

Claims 1, 4, 10, and 13 have been amended. Claims 1-18 remain in this application, of which claims 1 and 10 are independent claims.

Rejection of Claims 1-18 under 35 U.S.C. §102(e)

Claims 1-18 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application No. 2005/0024943 to Chen et al. (hereafter referred to as "Chen"). Applicants respectfully traverse this rejection.

Claims 1 and 10 have been amended to recite that (100%-X%) of the program verify level is at least a maximum potential change to a threshold voltage of a flash memory cell from programming any adjacent flash memory cells to the program verify level.

Figs. 8 and 9 and paragraphs [0055]-[0056] of Chen just discloses the threshold voltage distributions for programming the four multi-bit levels of "11", "10", "00", and "01". Thus, Chen does not even remotely mention that (100%-X%) of the program verify level is at least a maximum potential change to a threshold voltage of a flash memory cell from programming any adjacent flash memory cells to the program verify level.

The reason why Chen does not disclose, teach, or suggest such a limitation is because Figs. 8 and 9 and paragraphs [0055]-[0056] of Chen is directed toward just programming the four multi-bit levels. In contrast, the Present Invention is directed toward avoiding programming a flash memory cell beyond the program verify level in the first place, which Chen does not even remotely mention.

Anticipation of a claimed invention requires the presence in a single prior art document of ***each and every*** element of the properly construed claim. The Federal Circuit has set out the following requirements for anticipation pursuant to 35 U.S.C. §102:

> ...that a patent claim is anticipated under 35 U.S.C. §102 "must demonstrate, among other things, identity of invention."...[O]ne who seeks such a finding must show that each element of the claim in issue is found, either expressly or under principles of inherency, in a single prior art reference, or that the claimed invention was previously known or embodied in a single prior art device or practice.

Minnesota Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 1565 (Fed. Cir. 1992).

Because Chen does not disclose, teach, or suggest all of the limitations of amended claims 1 and 10, the rejection of claims 1 and 10 under 35 U.S.C. §102(e) in view of Chen should be withdrawn.

If the Examiner disagrees that Chen does not disclose, teach, or suggest all of the limitations of claims 1 and 10, the Examiner is respectfully requested to point out ***exactly where***, including ***specific column(s), line number(s), and figure element(s)*** in Chen, such a disclosure or suggestion may be found for (100%-X%) of the program verify level being at least a maximum potential change to a threshold voltage of a flash memory cell from programming any adjacent flash memory cells to the program verify level.

In addition, U.S. Patent Application No. 2003/0137888 to Chen et al. and U.S. Patent No. 6,456,528 to Chen are also directed to programming the four multi-bit levels, and thus also do not even remotely mention the limitation that (100%-X%) of the program verify level is at least a maximum potential change to a threshold voltage of a flash memory cell from programming any adjacent flash memory cells to the program verify level.

Claims 2-9 which depend from and further limit claim 1, are allowable for at least the same reasons that claim 1 is allowable as stated above.

Claims 11-18 which depend from and further limit claim 10, are allowable for at least the same reasons that claim 10 is allowable as stated above.

In addition, claims 4 and 13 have been amended to recite that (100%-Y%) of the first program verify level and (100%-Z%) of the second program verify level are each at least a maximum potential change to a threshold voltage of a flash memory cell from programming any adjacent flash memory cells to ***a higher of the first and second program verify levels***. Chen does not even remotely mention such a limitation.

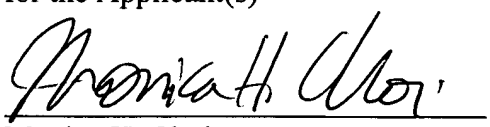
Furthermore, the Examiner does not address any of the limitations in the other dependent claims 2-3, 5-9, 11-12, and 14-18. For example, claims 8 and 17 recite the limitation that a page of the array is situated between V_{SS} (source bias voltage) lines and between drain bit line junctions. Chen does not even remotely mention such a limitation. The Examiner is respectfully requested to address all of the limitations of the dependent claims in rejecting such claims.

Conclusions

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. Please feel free to contact the undersigned should any questions arise with respect to this case that may be addressed by telephone.

Respectfully submitted,
for the Applicant(s)

Dated: August 19, 2005

By: 

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CERTIFICATE OF MAILING

The undersigned hereby certifies that the foregoing AMENDMENT AND RESPONSE is being deposited in the United States Postal Service, as first class mail, postage prepaid, in an envelope addressed to Commissioner for Patents, Box AF, P.O. Box 1450, Alexandria, VA 22313-1450, on this 19th day of August, 2005.

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